

REMARKS

Claims 1 – 12 are pending in the application. Applicants amend claims 1 and 8. No new matter is added. Support may be found, for example, at page 12, line 36 – page 13, line 21 and page 35, lines 7 - 35 of Applicants' specification.

REJECTION UNDER 35. U.S.C. §§ 102, 103

Claims 1 and 2 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,145,686 to McMurray et al. Claims 3 - 7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over McMurray in view of U.S. Patent No. 6,519,225 to Angle. Claims 8 – 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over McMurray in view of U.S. Patent No. 5,732,233 to Klim et al. Claims 11 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over McMurray in view of U.S. Patent No. 6,081,538 to Donley. Applicants amend claims 1 and 8 to clarify the nature of their invention, and respectfully traverse these rejections.

In independent claim 1, Applicants disclose:

1. A packet data processing apparatus for processing a packet received from a network by a processor, comprising:

a packet data access part, which has a plurality of registers arranged in series, shifting the received packet through the plurality of registers toward an outlet in synchronization with a clock,

wherein:

the processor processes the received packet while the received packet is being shifted through the plurality of registers, independently of an instruction order for processing the received packet;

the processor and the packet data access part are directly connected;

the processor reads out or writes data from or to the packet data access part by synchronizing the cycle time of the processor; and

each of the plurality of registers of the packet data access part is connected to a neighbor register via a selector which selects write data from the processor or the neighbor register.

McMurray discloses a data compressor for eliminating trains of redundant signals (see, e.g., abstract of McMurray). With reference to FIG. 1 of McMurray, the Examiner suggests that memory 28 corresponds to Applicants' claimed packet "data access part [having] a plurality of registers arranged in series". The Examiner further suggests that multiplexer 33 and /or sequencer 41 of FIG. 1 function to meet Applicants' claim limitations for "shifting [a] received packet through the plurality of registers toward an outlet in synchronization with a clock" and "processing the received packet while the received packet is being-shifted through the plurality of registers, independently of an instruction order for processing the received packet".

Applicants amend independent claim 1 to further require that "each of the plurality of registers of the packet data access part is connected to a neighbor register via a selector which selects write data from the processor or the neighbor register", and make the following clarifying distinctions between Applicants' claimed invention and the data compressor disclosed by McMurray.

In sharp contrast to Applicants' claimed invention of amended independent claim 1, neither multiplexer 33 nor sequencer 41 is able to write data to the memory 28 that is synchronized with a clock. Sequencer 41 provides no more than a clock pulse via line 56 to memory 28.

In addition, Applicants respectfully submit that, McMurray fails to disclose memory 28 of the data compressor as including Applicants' claimed plurality of registers each "connected to a neighbor register via a selector which selects write data from the processor or the neighbor register".

As described for example at page 13, lines 3 to 14 of Applicants' specification, each selector selects either a) processed "write data" from operation part 35 to be inserted into the data stream, or b) data from an upstream neighbor register ("neighbor register being bigger in number") to be shifted to a downstream neighbor register. In this manner, processing of data for a portion of the data stream can be performed in parallel with data shifting through the plurality of registers, and processed data can be inserted into an appropriate segment of the data stream through selection of an appropriate one of the plurality of selectors of the packet data access part (see, e.g., packet access register unit 32 as illustrated in Applicants' FIG. 3).

Accordingly, Applicants respectfully submit that amended independent claim 1 is not anticipated by McMurray, and is therefore in condition for allowance. Applicants essentially re-apply the above arguments with reference to amended independent claim 8, which effectively claims a plurality of packet data processing apparatuses as described in claim 1. Applicants respectfully submit that the addition of Klim to McMurray fails to suggest Applicants' claimed plurality of registers each connected to a neighbor register via a selector, that amended independent claim 8 is accordingly not obvious in view of these references, and that amended independent claim 8 is therefore in condition for allowance.

As claims 2 – 7 and 9 – 12 each depend from one of allowable claims 1 and 8, Applicant respectfully submits that claims 2 – 7 and 9 – 12 are also allowable for at least this reason.

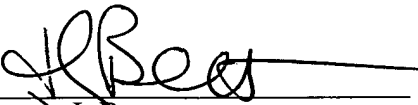
CONCLUSION

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that claims 1 – 12, consisting of independent claims 1 and 8, and the claims dependent therefrom, are in condition for allowance. Passage of this case to allowance is earnestly solicited. However, if for any reason the Examiner

should consider this application not to be in condition for allowance, she is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged on Deposit Account 50-1290.

Respectfully submitted,



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